FORM PTO-1390 (REV. 9-2001) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY 'S DOCKET NUMBER	
INF 4384	
U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	
Not yet assigned 09/980222	

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/SG99/00050	31 May 1999	

TITLE OF INVENTION
A METHOD OF ASSEMBLING A SEMICONDUCTOR DEVICE PACKAGE

APPLICANT(S) FOR DO/EO/US
Charles Lee and Helmut Strack

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [X] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [X] is attached hereto (required only if not communicated by the International Bureau).
   b. [ ] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [ ] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [ ] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [X] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [X] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). (unexecuted)
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [ ] Other items or information:

JC10 Rec'd PCT/PTO 29 NOV

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/980022 Not yet assigned	PCT/SG99/00050	INF 4384

21. ☒ The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 1,040.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$
Total claims	12 - 20 =		x **$18.00**	$
Independent claims	02 - 3 =		x **$84.00**	$
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$

TOTAL OF ABOVE CALCULATIONS =	$	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2. +	$	
SUBTOTAL =	$ 1,040.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).	$	
TOTAL NATIONAL FEE =	$ 1,040.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$	
TOTAL FEES ENCLOSED =	$ 1,040.00	
	Amount to be refunded:	$
	charged:	$

a. ☒ A check in the amount of $ 1,040.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-1345 . A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

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SIGNATURE

Robert M. Bain
NAME

36,736
REGISTRATION NUMBER

APPLICATION DATA SHEET

Application Information

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Subject Matter::	Utility
Suggested Classification::	
Suggested Group Art Unit::	
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Request for Non-Publication?::	No
Suggested Drawing Figure::	
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Small Entity?::	No

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Correspondence Information

Correspondence Customer Number:: 000321

Representative Information

Representative Customer Number:: 000321

Foreign Priority Information

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PCT	PCT/SG99/00050	05/31/1999	Yes

Assignee Information

Assignee Name:: Infineon Technologies AG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Lee et al.
Application No. Not Yet Assigned
Filing Date November 16, 2001
For A METHOD OF ASSEMBLING A SEMICONDUCTOR DEVICE PACKAGE

November 29, 2001

PRELIMINARY AMENDMENT A

TO THE ASSISTANT COMMISSIONER FOR PATENTS,

SIR:

Please enter the following amendments prior to examination of the above-referenced application:

IN THE CLAIMS:

Please amend claims 3, 4, and 8-12 as follows:

3. A method according to claim 1, wherein the semiconductor device package is a surface mount semiconductor device package.

4. A method according to claim 1, further comprising, after encapsulating the coated device/leadframe assembly, removing the coating from non-encapsulated portions of the leadframe.

8. A semiconductor device package according to claim 5, wherein the semiconductor device is attached to the first portion of the leadframe by an adhesive.

9. A semiconductor device package according to claim 5, wherein the semiconductor device is attached to the first portion of the leadframe by solder.

10. A semiconductor device package according to claim 5, wherein the semiconductor device is a surface mount semiconductor device.

11. A semiconductor device package according to claim 5, wherein the semiconductor device is a power semiconductor device.

12. A semiconductor device package according to claim 5, wherein the first portion of the leadframe forms a heat sink for the semiconductor device and a surface of the first portion is not covered by the electrically insulating material.

REMARKS

Applicant requests the entry of Preliminary Amendment A prior to the first Office action on the merits of the application. This Amendment amends the claims to avoid incurring fees for multiple dependent claims. Claims 3, 4, and 8-12 have been amended by this Amendment. Attached hereto is a marked-up version of the changes made to the claims by this Amendment. The attached page is captioned "Version With Markings To Show Changes Made."

The Commissioner is hereby authorized to charge any fees that may be required during the entire pendency of this application to Deposit Account No. 19-1345.

Respectfully submitted,

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Express Mail Label No. EV 015170880 US

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 3, 4, and 8-12 have been amended as follows:

3 (amended). A method according to claim 1 [or claim 2], wherein the semiconductor device package is a surface mount semiconductor device package.

4 (amended). A method according to [any of the preceding claims,] claim 1, further comprising, after encapsulating the coated device/leadframe assembly, removing the coating from non-encapsulated portions of the leadframe.

8 (amended). A semiconductor device package according to [any of claims 5 to 7] claim 5, wherein the semiconductor device is attached to the first portion of the leadframe by an adhesive.

9 (amended). A semiconductor device package according to [any of claims 5 to 7] claim 5, wherein the semiconductor device is attached to the first portion of the leadframe by solder.

10 (amended). A semiconductor device package according to [any of claims 5 to 9] claim 5, wherein the semiconductor device is a surface mount semiconductor device.

11 (amended). A semiconductor device package according to [any of claims 5 to 10] claim 5, wherein the semiconductor device is a power semiconductor device.

12 (amended) A semiconductor device package according to [any of claims 5 to 11] claim 5, wherein the first portion of the leadframe forms a heat sink for the semiconductor device and a surface of the first portion is not covered by the electrically insulating material.

A METHOD OF ASSEMBLING A SEMICONDUCTOR DEVICE PACKAGE

The invention relates to a method of assembling a semiconductor device package and in particular, a method of assembly which minimises or prevents delamination at interfaces within the assembled package.

Plastic surface mount semiconductor device packages are susceptible to cracking during solder reflow and this phenomenon is commonly referred to as "popcorn cracking". Popcorn cracking occurs because epoxy molding compounds used to encapsulate semiconductor devices are hygroscopic and readily absorb moisture from the environment. During solder reflow, high hydrothermal stresses are induced due to the combination of rapid vaporization of the absorbed moisture and mismatches in the coefficients of thermal expansion between dissimilar materials in the package. Once the stress level reaches a critical threshold, delamination occurs, usually at the weakest interface, followed by the build-up of vapour pressure in the delaminated cavity forming a characteristic dome-shaped bulge. This leads finally to cracking of the encapsulation material.

Popcorn cracking is a potential reliability problem as the delaminated areas and/or cracks can induce corrosion failures, alter the thermal performance of power devices, and affect the stress distribution and concentration.

The molding compound/die-pad interface is known to be susceptible to delamination and the source of most popcorn failure modes. The situation is aggravated with the emergence of larger and thinner packages. Moreover, moisture can degrade the polymer/metal interfacial durability, and decrease the fracture toughness of the molding compound at reflow temperatures. Furthermore, the oxidation of copper-based leadframe materials during the assembly process can result in poor adhesion between the molding compound and die-pad. The main cause of poor adhesion has been attributed to the weak copper oxide layer on the leadframe surface. Studies have reported that the adhesion strength between the molding compound and the copper leadframe decreases with increasing oxide thickness.

Various techniques to enhance molding compound/die-pad adhesion have been suggested as possible solutions to prevent popcorn cracking. However, most of the solutions which have been proposed do not eliminate the problem of popcorn cracking completely and are either not economically viable and/or feasible to implement in mass production.

For example, organic adhesion promoters such as silane coupling agents are widely used in die-attach adhesives and molding compounds to improve adhesion at the various interfaces. However, they are temperature sensitive and susceptible to degradation at elevated temperatures (typically greater than 200°C), for example, during wire

bonding.

Use of an inorganic zinc-chromium (Zn-Cr) leadframe coating (commercially known as "Olin A2" and supplied by Olin Metal Research Laboratories) is believed to be effective in eliminating popcorn cracking. However, the Zn-Cr coating is deposited on the leadframe electrolytically via an electroplating process. However, due to the temperature stability of the Zn-Cr coating layer, it can prevent or interfere with subsequent solid-state bonding, fusion or soldering processes such as wire bonding, etc. Therefore, it is necessary to either mask the bonding/soldering areas during the coating process or to subsequently strip the coating from these areas. Therefore, there are surfaces of the leadframe and semiconductor device in the finished package which do not have the Zn-Cr coating and are still prone to popcorn cracking.

Chip buffer coatings such as polyimides, are commonly used to minimise thermo-mechanical stresses and delamination at the mold compound/chip interface. However, polyimides have the disadvantage that they have a tendency to absorb moisture and therefore, further contribute to popcorn cracking.

In accordance with a first aspect of the present invention, a method of assembling a semiconductor device package comprises:

(i) attaching a semiconductor device to a die-pad area of a leadframe;

(ii) forming electrical connections between electrical contact areas on the semiconductor device and electrical contact areas on the leadframe to form a device/leadframe assembly;

(iii) depositing an adhesion enhancing coating on exposed surfaces of the device/leadframe assembly; and

(iv) encapsulating the coated device/leadframe assembly in an electrically insulating material.

In accordance with a second aspect of the present invention, a semiconductor device package comprises a leadframe; a semiconductor device attached to a first portion of the leadframe; electrical connections extending from electrical contact areas on the semiconductor device to electrical contact areas on a second portion of the leadframe; an adhesion enhancing coating on surfaces of the leadframe, the electrical connections and the semiconductor device; and an electrically insulating material encapsulating the semiconductor device, the electrical connections and the first and second portions of the leadframe.

An advantage of the invention is that by depositing an adhesion enhancing coating on the leadframe and semiconductor device after the electrical connections are formed between the semiconductor device and the leadframe,

the adhesion enhancing coating is also deposited on the electrical connections between the semiconductor device and the leadframe. There is also the advantage that if the adhesion enhancing coating is deposited electrolytically via an electroplating process, the electrical connections provide a conduction path from the leadframe to the semiconductor device to enable electrolytic deposition of the adhesion enhancing coating on electrically conducting surfaces of the semiconductor device.

Preferably, the adhesion enhancing coating is a metallic coating and is typically deposited electrolytically via an electroplating process.

Preferably, the metallic coating is an inorganic Zn-Cr coating, such as Olin A2.

Typically, the semiconductor device may be attached to the leadframe by an epoxy die-attach adhesive or with solder die-attach.

Preferably, the semiconductor device package is a surface mount semiconductor device package.

An example of a method of assembling a semiconductor device package in accordance with the invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a cross-sectional view through a surface mount semiconductor device package having an adhesion enhancing coating in accordance with the prior art;

Figure 2 is a cross-sectional view through a surface mount semiconductor device package in which a semiconductor device is attached to a leadframe with epoxy die-attach adhesive and incorporating an adhesion enhancing coating in accordance with the invention;

Figure 3 is a cross-sectional view through a surface mount semiconductor package in which a semiconductor device is attached to a leadframe with solder and incorporating an adhesion enhancing coating in accordance with the invention; and

Figure 4 is a cross-sectional view through a surface mount semiconductor package including a power semiconductor device with a protruding heat sink.

Figure 1 is a cross-sectional view through a surface mount semiconductor device package 1 in which a leadframe 2, which comprises a die-pad area 2a and bonding leads 2b, has been coated with a Zn-Cr coating 3 (such as Olin A2) which is deposited on the leadframe electrolytically via an electroplating process prior to attachment of a semiconductor device 4 to the die-pad area 2a.

During deposition of the coating 3 it is necessary to either mask bonding areas 7 of the bonding leads 2b to

which the wires 5 are to be bonded, or to carry out the deposition of the Zn-Cr coating 3 by a two step plate and strip process. Generally it is also necessary to mask or strip a portion of the die-pad area 2a to permit establishment of an electrical ground contact between the semiconductor device 4 and the die-pad area 2a.

After the masking has been removed from the leadframe 2, or the coating 3 has been stripped from the relevant areas, the semiconductor device 4 is attached to the die-pad portion 2a by an epoxy die-attach adhesive 6. The leadframe 2 with the semiconductor device 4 attached is then passed to a wire bonding process in which wires 5 are bonded between the bonding areas 7 on the bonding leads 2b and electrical contact areas on the semiconductor device 4.

Generally, the leadframe 2 is only one of a number of leadframes 2 which are joined together to form of a strip or matrix of leadframes 2. Each leadframe 2 on the strip or matrix comprises a die-pad area 2a and respective bonding leads 2b. Each die-pad area 2a on the leadframe 2 will have a semiconductor device 4 attached to it by a die-attach adhesive 6. Having the leadframes 2 in a strip or matrix which carries a number of semiconductor devices 4 permits easier handling of the leadframes 2 during assembly of the semiconductor device package 1.

After the wire bond process, the strip or matrix of

leadframes 2 is passed to a molding process where an electrically insulating encapsulation material 8 is molded around the die-pad area 2a, bonding areas 7, semiconductor device 4 and wires 5 to leave only extremities of the bonding leads 2b protruding from the encapsulation material 8.

After the molding process, the leadframes 2 are singulated to separate each semiconductor device 4 and the respective die-pad area 2a and bonding leads 2b from adjacent semiconductor devices 4 and respective die-pad areas 2a and bonding leads 2b. Optionally, after the molding process, the coating can be removed from the extremities of the bonding leads 2b and/or from a protruding heat sink (if present).

There are a number of disadvantages associated with this prior art coating process. In particular, the requirement to either mask portions of the leadframe 2 or to subsequently strip coating from areas such as the bonding areas 7 and the ground bond area on the die-pad area 2a. In addition, this prior art coating process cannot coat the surface of the semiconductor device 4. Hence, this conventional assembly method does not prevent delamination and subsequent popcorn cracking at interface 9 between the molding compound 8 and the semiconductor device 4.

Figure 2 shows a cross-sectional view of a semiconductor

device package 10 which includes the same components as the semiconductor device package 1 and the same items are identified using the same reference numerals as in Figure 1. However, the process for assembly of the semiconductor device package 10 is slightly different from that used for the semiconductor device package 1 shown in Figure 1.

In the assembly of the package 10, the semiconductor device 4 is attached to the die-pad portion 2a by an epoxy die-attach adhesive 6 before the Zn-Cr coating 3 is deposited. As in the example described above, the leadframe 2 is initially one of a number of leadframes 2 joined together to form a strip or matrix. After the semiconductor device 4 has been attached to the die-pad portion 2a, the strip or matrix of leadframes 2 with the attached semiconductor devices 4 is passed to a wire bonding process for bonding of the wires 5 between contact areas on the semiconductor device 4 and the bonding areas 7 on the bonding leads 2b.

After the wire bonding process, the strip or matrix of leadframes 2, with the attached semiconductor device 4 and the wire bonds 5, is immersed in an electroplating bath and the Zn-Cr coating 3 is deposited electrolytically on the leadframe 2 in the areas shown, on the wire bonds 5 and electrically conducting surfaces on the semiconductor device 4 by an electroplating process.

After deposition of the Zn-Cr coating 3, the electrically

insulating encapsulation material 8 is molded around the semiconductor devices 4, leadframes 2 and wire bonds 5, as in the prior art package 1. The strip or matrix of leadframes 2 is then singulated into individual semiconductor device packages.

Figure 3 shows a semiconductor device package 30 which has been assembled using a process similar to that used for assembly of the semiconductor device package 10. However, the semiconductor device 4 is attached to the die-pad area 2a by solder 31. Therefore, as the solder 31 is electrically conducting, the Zn-Cr coating 3 is also deposited along the sides of the solder 31.

Figure 4 shows a semiconductor device package 40 which has been assembled using a process similar to that used for assembly of the semiconductor device packages 10, 30. However, the package 40 includes a power semiconductor device 41 attached to a thickened die-pad area 2a by solder 31. Therefore, as the solder 31 is electrically conducting, the Zn-Cr coating 3 is deposited along the sides of the solder 31, as in the package 30. In addition, as a bottom surface 43 of the die-pad area 2c is not covered by the material 8, and the solder 31 is thermally conductive, the die pad area 2c acts as a heat sink for the device 41.

In the device packages 10, 30, 40, the coating is removed

from non-encapsulated portions of the leadframe 2. In the packages 10, 30 the coating is removed from the non-encapsulated portions of the bonding leads 2b and in the package 40 the coating is removed from the non-encapsulated portions of the bonding leads 2b and the surface 43 of the die-pad area 2c. However, removal of the coating from these areas is not essential and is only a possible option.

By depositing the Zn-Cr coating 3 after attachment of the semiconductor devices 4, 41 to the die-pad areas 2a, 2c of the leadframe 2 and formation of the wire bonds 5, it is not necessary to mask any areas of the leadframe 2 during the coating process.

In addition, by depositing the coating 3 after wire bonding, but before molding, there is the advantage that the entire wire bonded assembly is submerged into the plating bath for coating deposition, and as the wires 5 establish electrical paths from the leadframe 2 to the electrical contact surfaces of the semiconductor device 4, the Zn-Cr coating 3 is also deposited on the electrical contact surfaces of the semiconductor device 4. The degree of coating coverage on the surface of the device 4 is dependent on the availability of electrically conducting paths on the surface. This is influenced by device design, distribution of metallisation, type of device passivation, provision of intrinsic/extrinsic passivation and provision of intrinsic/extrinsic electrical contact.

As an alternative to electrolytical deposition, it is possible that the coating could be deposited by a wet chemical catalytic process or a dry, physical/chemical deposition. In addition, although the deposition of a Zn-Cr coating has been described any metallic or non-metallic coating could be deposited using the invention.

Claims

1. A method of assembling a semiconductor device package comprises:

(i) attaching a semiconductor device to a die-pad area of a leadframe;

(ii) forming electrical connections between electrical contact areas on the semiconductor device and electrical contact areas on the leadframe to form a device/leadframe assembly;

(iii) depositing an adhesion enhancing coating on exposed surfaces of the device/leadframe assembly; and

(iv) encapsulating the coated device/leadframe assembly in an electrically insulating material.

2. A method according to claim 1, wherein the adhesion enhancing coating is deposited electrolytically by an electroplating process.

3. A method according to claim 1 or claim 2, wherein the semiconductor device package is a surface mount semiconductor device package.

4. A method according to any of the preceding claims, further comprising, after encapsulating the coated device/leadframe assembly, removing the coating from non-encapsulated portions of the leadframe.

5. A semiconductor device package comprises a leadframe; a semiconductor device attached to a first portion of the leadframe; electrical connections extending from electrical contact areas on the semiconductor device to electrical contact areas on a second portion of the leadframe; an adhesion enhancing coating on surfaces of the leadframe, the electrical connections and the semiconductor device; and an electrically insulating material encapsulating the semiconductor device, the electrical connections and the first and second portions of the leadframe.

6. A semiconductor device package according to claim 5, wherein the adhesion enhancing coating is a metallic coating.

7. A semiconductor device package according to claim 6, wherein the metallic coating is an inorganic Zn-Cr coating.

8. A semiconductor device package according to any of claims 5 to 7, wherein the semiconductor device is attached to the first portion of the leadframe by an adhesive.

9. A semiconductor device package according to any of claims 5 to 7, wherein the semiconductor device is attached to the first portion of the leadframe by solder.

10. A semiconductor device package according to any of claims 5 to 9, wherein the semiconductor device is a

surface mount semiconductor device.

11. A semiconductor device package according to any of claims 5 to 10, wherein the semiconductor device is a power semiconductor device.

12. A semiconductor device package according to any of claims 5 to 11, wherein the first portion of the leadframe forms a heat sink for the semiconductor device and a surface of the first portion is not covered by the electrically insulating material.

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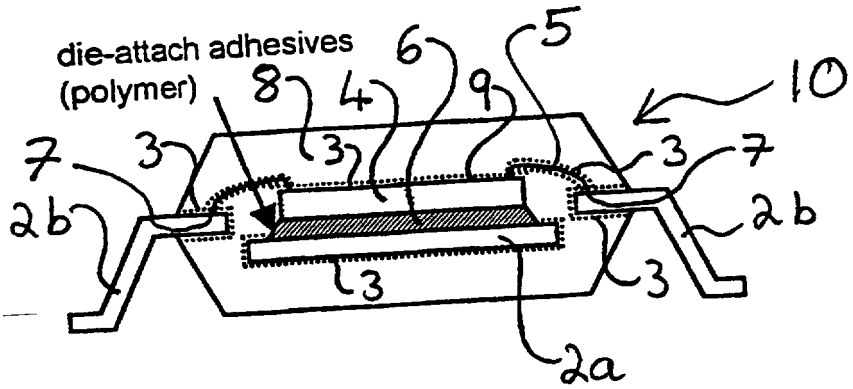
(54) Title: A METHOD OF ASSEMBLING A SEMICONDUCTOR DEVICE PACKAGE



(57) Abstract: A method of assembling a semiconductor device package (10) includes first attaching a semiconductor device (4) to a die-pad area (2a) of a leadframe (2). Electrical connections (5) are then formed between electrical contact areas on the semiconductor device (4) and electrical contact areas (7) on the leadframe (2) to form a device/leadframe assembly (2, 4, 5). An adhesion enhancing coating (3) is then deposited on exposed surfaces of the device/leadframe assembly (2, 4, 5) before encapsulating the device/leadframe assembly (2, 4, 5) in an electrically insulating material.

WO 00/74131 A1

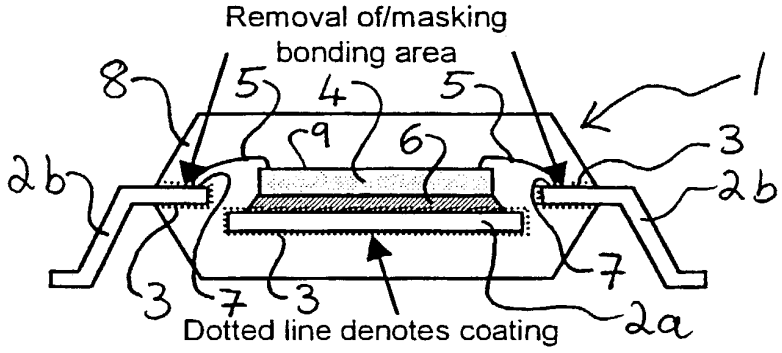


Figure 1

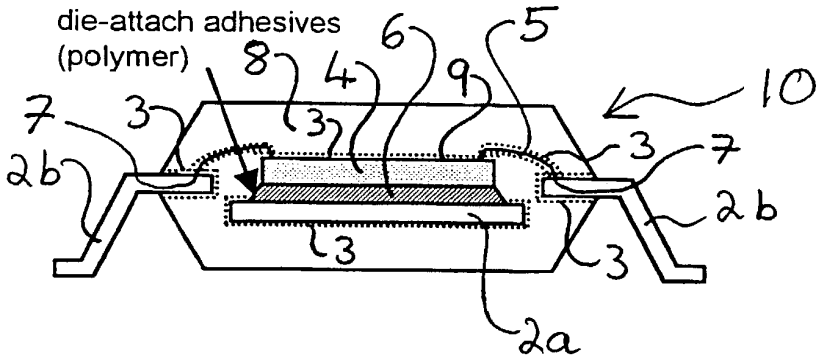


Figure 2

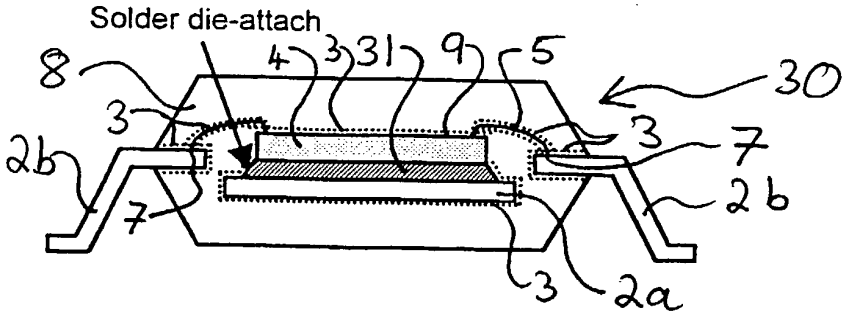


Figure 3

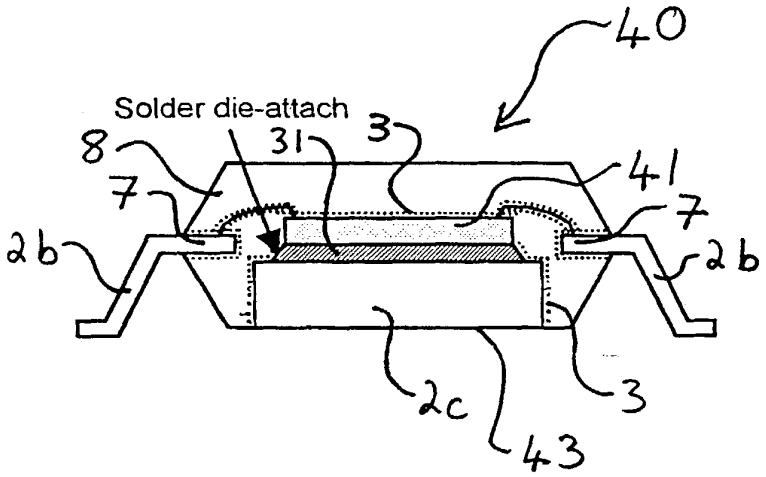


Figure 4

Attorney's Docket No. INF 4384

DECLARATION AND POWER OF ATTORNEY

REGULAR OR DESIGN APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A METHOD OF ASSEMBLING A SEMICONDUCTOR DEVICE PACKAGE

the specification of which:

[ ] is attached hereto
[X] was filed on 11/29/01 as Application Serial No. 09/980,222, and was amended on _____.
[X] was described and claimed in PCT International Application No. PCT/SG99/00050, filed on 31 May 1999 and as amended under PCT Article 19 on _____, if any.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a) - (d) or §365(b) of any foreign application for patent or inventor's certificate, or §365(a) of any PCT application which designates at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Priority Claimed

(Number)	(Country)	(Day/Month/Year Filed)
(Number)	(Country)	(Day/Month/Year Filed)
(Number)	(Country)	(Day/Month/Year Filed)

Priority Not Claimed

ANY FOREIGN APPLICATION(S), ON THE SAME SUBJECT MATTER WHICH HAS A FILING DATE EARLIER THAN THE EARLIEST APPLICATION FROM WHICH PRIORITY IS CLAIMED

(Number)	(Country)	(Day/Month/Year Filed)

CLAIM FOR BENEFIT OF PROVISIONAL APPLICATION(S)

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

CLAIM FOR BENEFIT OF EARLIER U.S. APPLICATION(S) UNDER 35 U.S.C. 120

(complete this part only if this is a divisional, continuation or CIP application)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or §365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Serial No.)	(Filing Date)	(Status)
(Serial No.)	(Filing Date)	(Status)

POWER OF ATTORNEY

I hereby appoint the following attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Irving Powers (15,700), Donald G. Leavitt (17,626), John K. Roedel, Jr. (25,914), Michael E. Godar (28,416), Edward J. Hejlek (31,525), William E. Lahey (26,757), Richard G. Heywood (18,224), Frank R. Agovino (27,416), Kurt F. James (33,716), G. Harley Blosser (33,650), Paul I. J. Fleischut (35,513), Vincent M. Keil (36,838), Robert M. Evans, Jr. (36,794), Robert M. Bain (36,736), Kathleen M. Petrillo (35,076), David E. Crawford, Jr. (38,118), Richard L. Bridge (40,529), Christopher M. Goff (41,785), Derick E. Allen (43,468), Michael G. Munsell (43,820), Anthony R. Kinney (44,834), Brian P. Klein (44,837), Sarah J. Chickos (46,157), Donald W. Tuegel (45,424), Steven M. Ritchey (46,321), Michael J. Thomas (39,857), Kathryn J. Doty (40,593), Laura R. Polcyn (47,000), James J. Barta, Jr. (47,409), John M. Bodenhausen (47,432), James E. Davis (47,516), Richard A. Schuth (47,929), Debra D. Nye (48,260), Jennifer E. Hoekel (P-48,330) and Timothy B. McBride (47,781), all of the law firm of SENNIGER, POWERS, LEAVITT & ROEDEL, One Metropolitan Square, 16th Floor, St. Louis, Missouri 63102.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

- -

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

- -

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